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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/559,757	04/27/00	OZAWA	Y 04329.2306

EXAMINER	
MONDT, J	
ART UNIT	PAPER NUMBER
2826	

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DATE MAILED: 10/10/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/559,757	OZAWA ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-7 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-7 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

The examiner has considered the items listed in the Information Disclosure Statement.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. *Claims 1-4 are rejected* under 35 U.S.C. 103(a) as being unpatentable over Rhee (5,646,054) in view of Teramoto (5,620,910).

With regard to claim 1, and with reference to Fig. 7: Rhee teaches a MOS transistor, which is a semiconductor device, comprising:

(a) a semiconductor substrate 42 (column 4, lines 1-2) having a main plane which has a first region, bordering gate insulation film 60, and a second region, bordering oxide film 80; said second region having a surface that is lower than the surface of the first region, as evidenced by Fig. 7. Furthermore, the first region and the second region are connected to each other, because region 42 is contiguous. Also:

(b) a first insulating film 60 is formed on the first region (see column 4, lines 4-5);

(c) a conductive film 62 containing silicon (in fact: made of polysilicon; see column 4, lines 5-6) is formed on the first insulating film 60; and

(d) a second insulating film 80 (column 7, lines 13-14), containing oxygen and arranged to be in contact with both the conductive film 62 and the first insulating film 60 (cf. Fig.7), is formed on the second region of the semiconductor substrate 42.

Rhee does not specifically teach the first insulating film to contain silicon, nitrogen and oxygen to take advantage of the dielectric properties of such materials, nor does Rhee teach the second insulating oxide film to contain silicon to take advantage of the good electrical insulation properties found among materials comprising both silicon and oxide. However, silicon oxynitride, a substance containing silicon, nitrogen and oxygen, has long been recognized for its excellent dielectric strength properties in connection with gate insulation layers, as evidenced by Teramoto, who teaches the application of SiO_xN_y as a thin gate insulation layer 506 (cf. Figs. 10C,F and column 18, lines 37-38); while Teramoto uses silicon oxide for the other insulation layers. The examiner takes official notice that the use of silicon dioxide for field oxide components in the art of semiconductor devices has been well known to those of ordinary skills in the art for a long time. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention by Rhee at the time it was made so as to include silicon, nitrogen, and oxygen in the first insulation film, and so as to include silicon and oxygen in the second insulation film.

With regard to the further limitation of *claims 2 and 3:* as detailed above, Rhee does not teach the first insulating film to contain nitrogen, and therefore, *a forteriori,* Rhee does not teach a portion of said first insulating film that is in contact with the semiconductor substrate to contain nitrogen at a concentration higher than the concentration in a residual portion of the first insulating film, so as to create a barrier layer within the gate insulation film. However, Teramoto teaches (see Fig. 6) a nitrogen concentration profile in the gate insulation film 306 (506) that is higher in a portion of 306 (506) that is in contact with the (active layer of the) semiconductor substrate 304 (504) than it is in a residual portion in the mid section of said first insulating film alias gate insulating film (see column 12, lines 1-8). Parenthetically it is noted that the active layer is part of the substrate by virtue of functional necessity. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention of Rhee at the time it was made so as to include a nitrogen concentration profile within the gate insulation layer (first insulating layer of Applicant) such that said concentration is higher in a portion that is in contact with the semiconductor substrate than in a residual portion of the gate insulation layer (first insulating layer of Applicant), that is: to incorporate Applicant's claim 2. The nitrogen concentration in the portion of the gate insulation film in contact with the semiconductor substrate as taught by Teramoto preferably ranges from 1 to atomic 30 %, and thus amply exceeds the limit of 5×10^{13} cm^{-2} for the concentration per unit surface of the interface. Thus, for the same reasons as given above, it would have been obvious to one of ordinary skills in the art to carry out abovementioned modification of the invention of Rhee in such as way as to select for

the concentration of nitrogen in a portion of the first insulating film in contact with the semiconductor substrate a value of 5 X 10^{13} cm^{-2} (*claim 3*).

With regard to claim 4: the examiner takes official notice that the function of nitrogen as used by Teramoto as detailed above under the discussion of claims 2 and 3 to create a diffusion barrier so as to prevent gate material to penetrate into the surrounding dielectric obviously has utility independent upon the direction into which said diffusion takes place, and that therefore the application of the same procedure as taught for the gate insulation film can be usefully inferred from the invention of Teramoto to be advantageous in the direction of the second insulating film as well. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention of Rhee so as to include nitrogen in the contents of the second insulting film (see claim 2) and such that a portion of the second insulating film that is in contact with the semiconductor substrate and the conductive film has a (nitrogen) concentration higher than the concentration in the residual portion of the second insulating film.

3. *Claims 5-6 are rejected* under 35 U.S.C. 103(a) as being unpatentable over Rhee and Teramoto as applied to claim 1 above, and further in view of Takemura (5,917,221). As detailed above, claim 1, on which claim 5 depends, is unpatentable over Rhee in view of Teramoto. Furthermore, the first insulating film taught by Teramoto is a silicon oxide film containing nitrogen. Neither Rhee nor Teramoto teach the conductive film to be made of a polycrystalline silicon film containing a dopant so as to increase the gate conductivity and thereby decrease the response time, although Rhee teaches the film to

be made of a polycrystalline silicon film. However, the use of dopants to this end is well known among those skilled in the art of active semiconductor devices, as evidenced by for instance Takemura, who teaches a field effect device with a phosphorus (n-type) doped polysilicon gate (see column 10, lines 22-27). Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention essentially taught by Rhee and Takemura so as to select a silicon oxide film containing nitrogen for the first insulating film and to include a conductive film of polycrystalline silicon containing a dopant.

With regard to claim 6: the first insulating film and conductive film as taught by Rhee and Teramoto are a gate insulating film and gate electrode, respectively (see discussion under claim 1).

4. *Claim7 is rejected* under 35 U.S.C. 103(a) as being unpatentable over Rhee, Teramoto and Takemura as applied to claim 5 above, and further in view of Tomita et al (5,959,329). As detailed above, claim 5 (on which claim 7 depends) is unpatentable over Rhee, Teramoto, and Takemura, who, however, do not teach the first insulating film as a tunnel gate insulating film to improve stress leak, dielectric breakage life, and charge trap amount characteristics, nor do they teach the conductive film as a floating electrode. However, silicon oxynitride tunnel gate insulating films are well-known in the art of oxide films for active semiconductor devices as shown by the U.S. Patent to Tomita et al, who teach a "tunnel oxide film" (see column 1, lines 6-8); however, the advantages of a silicon oxynitride film for the reasons given above (stress leak, dielectric breakage, charge trap amount characteristics) are clearly delineated (see

column 2, 3-8). The examiner takes official notice that the same obviousness considerations as given above apply to a floating gate electrode as to any other gate electrode, with regard to the desirable material characteristics of the gate and its insulating surroundings, i.e., irregardless of whether the voltage is driven or floating, as enumerated above. Therefore, it would have been obvious to one of ordinary skills in the art to modify the invention essentially taught by Rhee, Teramoto and Takemura at the time it was made so as to equip the semiconductor device of claim 5 with a tunnel gate insulating film as the first insulating film and a floating electrode as the conductive film.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
October 4, 2001

Nathan Flynn
Primary Examiner